

CLAIMS

What is claimed is:

1. A method for self-routing a packet to a given destination address through a
5 network, the network being characterized by a guide transform, the method comprising
generating a routing tag for the packet with reference to the guide transform
and the destination address, and
routing the packet through the network using the routing tag.
- 10 2. The method as recited in claim 1 wherein generating a routing tag includes
computing the guide transform of the destination address.
- 15 3. The method as recited in claim 2 wherein the destination address is expressed as
binary($d_1d_2\dots d_k$) and the guide transform is expressed as $\gamma(1), \gamma(2), \dots, \gamma(k)$, and wherein
the computing includes generating binary $(d_{\gamma(1)}d_{\gamma(2)}\dots d_{\gamma(k)})$.
4. The method as recited in claim 3 including prepending binary $(d_{\gamma(1)}d_{\gamma(2)}\dots d_{\gamma(k)})$
to the packet.

5. The method as recited in claim 4 wherein the network is an n-stage network composed of nodes, the guide transform is expressed as $\gamma(1), \gamma(2), \dots, \gamma(n)$ and wherein, for an j-th stage node, the routing includes using $d_{\gamma(j)}$ in the j-th stage node to select an output from the j-th stage node to emit the packet, $1 \leq j \leq n$.

5

6. A method for self-routing a packet through a $2^n \times 2^n$ switch, the switch having 2^n external output ports labeled with 2^n distinct binary output addresses in the form of $b_1b_2\dots b_n$, and is composed of a plurality of switching cells interconnected into a k-stage bit-permuting network which is characterized by the guide $\gamma(1), \gamma(2), \dots, \gamma(k)$ where γ is a mapping from the set $\{1, 2, \dots, k\}$ to the set $\{1, 2, \dots, n\}$, wherein each of the switching cells is a sorting cell associated with the partial order “0 (‘0-bound’) \prec 1 (‘1-bound’)\”, the packet being destined for a binary output address $d_1d_2\dots d_n$, the method comprising generating a routing tag $d_{\gamma(1)}d_{\gamma(2)}\dots d_{\gamma(k)}$ for the packet with reference to the guide and the destination output address of the packet, and routing the packet through the network by using $d_{\gamma(j)}$ in the routing tag in the j-th stage cell, $1 \leq j \leq k$, to select an output from the j-th stage cell to emit the packet.

7. The method as recited in claim 6 wherein the routing includes removing the bit

$d_{\gamma(j)}$ from the routing tag before the packet exits the j-th stage cell, $1 \leq j \leq k$.

8. The method as recited in claim 6 wherein the routing includes using the leading bit in the routing tag in the j-th stage cell, $1 \leq j \leq k$, to select an output from the j-th stage cell
5 to emit the packet.

9. The method as recited in claim 6 wherein the routing includes the removing the leading one bit from the routing tag of the packet before the packet exits the j-th stage cell, $1 \leq j \leq k$.
10

10. The method as recited in claim 6 wherein the switch is characterized as an n-stage banyan-type network with guide $\gamma(1), \gamma(2), \dots, \gamma(n)$, where γ is a permutation on the integers from 1 to n.

15 11. The method as recited in claim 6 wherein the packet is an idle packet which is a stream of '0' bits such that the packet is either a real data packet or an idle packet.

12. The method as recited in claim 6 wherein the sorting cell is associated with the

partial order “10 (‘0-bound’) < 00 (‘idle’) < 11 (‘1-bound’)”.

13. The method as recited in claim 6 wherein generating the routing tag includes

generating the routing tag $1d_{\gamma(1)}d_{\gamma(2)}\dots d_{\gamma(k)}$ for a real data packet.

5

14. The method as recited in claim 13 wherein the routing includes using $1d_{\gamma(j)}$ in

the routing tag of the real data packet in the j -th stage cell, $1 \leq j \leq k$, to select an output from
the j -th stage cell to emit the real data packet.

10

15. The method as recited in claim 14 wherein the routing includes removing the

bits $1d_{\gamma(i)}$ from the routing tag before the real data packet exits from the j -th stage cell,
 $1 \leq j \leq k$.

16. A $2^n \times 2^n$ self-routing switch having an array of 2^n external input ports and an

15 array of 2^n external output ports with 2^n distinct binary output addresses in the form of

$b_1b_2\dots b_n$ for switching a packet, the packet being either a real data packet destined for an
n-bit binary destination address, or being an idle packet having no pre-determined
destination output address, the switch comprising

a switch fabric with external input ports, the switch fabric having a plurality of switching cells interconnected into a k-stage bit-permuting network which is characterized by the guide $\gamma(1), \gamma(2), \dots, \gamma(k)$, where γ is a mapping from the set $\{1, 2, \dots, k\}$ to the set $\{1, 2, \dots, n\}$,

- 5** a routing tag circuit, coupled to the external input ports, for generating a routing tag $1d_{\gamma(1)}d_{\gamma(2)}\dots d_{\gamma(k)}$ for each of the real data packets with reference to the guide of the bit-permuting network and the destination output address of the packet, and
- 10** a routing control circuit, coupled to the switching cells, for routing the real data packet through the switch by using $1d_{\gamma(j)}$ in the routing tag of the packet in the j-th stage cell, $1 \leq j \leq k$, to select an output from the j-th stage cell to emit the packet.